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| 10/522,686 | 04/12/2005 | Hideo Kikuchi | DP-948 US | 9224 |

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| EXAMINER | |
|---|---|
| LEE, JINHEE J | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2831 | |

DATE MAILED: 12/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/522,686 | KIKUCHI ET AL. | |
| | Examiner | Art Unit | |
| | Jinhee J. Lee | 2831 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *0105, 0505*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Drawings*

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, (arranged on) both end sides (of the ceiling plate section) in a front-rear direction of the shielding conductor project from both side ends of the chip part, and electromagnetic wave absorber of claim 1, and two-terminal chip part of claim 2 must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Applicant is required to submit a proposed drawing correction in reply to this Office action. However, formal correction of the noted defect may be deferred until after the examiner has considered the proposed drawing correction. Failure to timely submit the proposed drawing correction will result in the abandonment of the application.

### *Specification*

3. The abstract of the disclosure is objected to because the reference characters are not in parenthesis. Correction is required. See MPEP § 608.01(b).

4. The disclosure is objected to because of the following informalities:

At page 11 line 14, "FIGS. 16A, 16B " is confusing. Clarify.

5. The specification is also objected because throughout the specification, the applicant has phrases like "....with one of claims 1 to 8", which is improper form for the

specification. The applicant is reminded that the claims are enabled by the specification and not vice versa. The applicant should delete the above phrases and all of the similar phrases referencing the claim numbers and specifically state what material the applicant is trying to specify.

### *Claim Objections*

6. Claims 17 and 18 are objected to because of the following informalities:

Claim 17 line 4 and claim 18 line 4, the phrase "characterized by comprising" has an error. Examiner suggests "comprising" instead to correct the error.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The limitation of harmonic mean is not adequately described in the specification.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 3, 5 and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 3 recites the limitation "between at least from the both side ends" in line 9-10. There is insufficient antecedent basis for "the both side ends" in the claim and the limitation is confusing.

Claim 5 recites the limitation "chip part exist" in line3-4. This is confusing. Clarify.

Claim 6 recites the limitation "the opening" in line 2-3. There is insufficient antecedent basis for this limitation in the claim.

***Claim Rejections - 35 USC § 102***

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claims 1, 2, 6, 7, 12 and 17-19 are rejected under 35 U.S.C. 102(b) as being anticipated by Nardoni et al. (EP000812015A1).

Re claim 1, Nardoni et al. discloses an electronic device characterized in that an upper surface of the chip part (IC) is coated with the shielding conductor (B), the shielding conductor includes a ceiling plate section (B) covering the chip part and side plate sections (D) which are formed to be united with the ceiling plate section and to be at a position lower than the ceiling plate section and which are arranged on both sides

in a horizontal direction of the chip part, side plates do not exist in both side ends in a front-rear direction of the shielding conductor, and the side plate sections are electrically connected via a plurality of connecting means (SBT for example) to a ground layer (PS) of a mounting substrate (P) (see figure 3).

Re claim 2, Nardoni et al. discloses an electronic device characterized in that the shielding conductor (B) includes a ceiling plate section (B) covering the chip part and side plate sections (D) which are formed to be united with the ceiling plate section and to be at a position lower than the ceiling plate section and which are arranged on both sides in a horizontal direction of the chip part, and openings are formed in both side ends in a front-rear direction of the shielding conductor to open both sides in a front-rear direction of the chip part, and the side plate sections of the shielding conductor are electrically connected via a plurality of connecting means (SBT for example) in the front-rear direction to the ground layer (PS) of the mounting substrate (P).

Re claim 6, Nardoni et al. discloses an electronic device, characterized in that in the shielding conductor, end sections of the opening (unnumbered) of the shielding conductor are of a size larger than an area in which terminals of the chip part exist, by at least length L of the opening in the horizontal direction of the ceiling plate section (see figure 3).

Re claim 7, Nardoni et al. discloses an electronic device, characterized in that more than four connecting means are used (see figures 2 and 3).

Re claim 12, Nardoni et al. discloses an electronic device, characterized in that a bump or a conductor having elasticity is used as the connecting means (see figures 2 and 3).

Re claim 17, Nardoni et al. discloses a method of manufacturing an electronic device comprising: a step of assembling the chip part with the shielding conductor (B) into a unit by using a shielding conductor (B) including a ceiling plate section (B) covering the chip part (IC) and side plate sections (D) which are formed to be united with the ceiling plate section and to be at a position lower than the ceiling plate section and which are arranged on both sides in a horizontal direction of the chip part and by coating an upper surface of the chip part with the ceiling plate section; and a step of using a mounting substrate (P) in which a ground layer is formed, arranging on the mounting substrate the shielding conductor assembled with the chip part into a unit, mounting the chip part on a surface of the mounting substrate, and electrically connecting the shielding conductor to the ground layer at the same time.

Re claim 18, Nardoni et al. discloses a method of manufacturing an electronic device comprising: a step of using a mounting substrate in which a ground layer (PS) is formed, arranging the chip part (IC) on the mounting substrate (P) , and mounting the chip part on a surface of the mounting substrate; and a step of using a shielding conductor (B) including a ceiling plate section (B) covering the chip part and side plate sections (D) which are formed to be united with the ceiling plate section and to be at a position lower than the ceiling plate section and which are arranged on both sides in a horizontal direction of the chip part, arranging the shielding conductor on the mounting

substrate, electrically connecting the shielding conductor to the ground layer, and covering an upper surface of the chip part with the ceiling plate section.

Re claim 19, Nardoni et al. discloses a method of manufacturing an electronic device comprising, characterized in that a plurality of connecting means (SBT) are used when the shielding conductor is electrically connected to the ground layer.

***Claim Rejections - 35 USC § 103***

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 3-5, 8-10, 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nardoni et al.

Re claim 3, Nardoni et al. substantially discloses an electronic device characterized in that the shielding conductor includes a ceiling plate section covering

the chip part and side plate sections which are formed to be united with the ceiling plate section and to be at a position lower than the ceiling plate section and which are arranged on both sides in a horizontal direction of the chip part, and the side plate sections of the shielding conductor are electrically connected via a plurality of connecting means in the front-rear direction to the ground layer of the mounting substrate. Nardoni et al. does not explicitly disclose the ceiling plate section which are arranged on both end sides in a front-rear direction of the shielding conductor project from both side ends of the chip part, and an electromagnetic wave absorber is disposed between at least from the both side ends in a front-rear direction of the chip part to the both side ends in a front-rear direction of the shielding conductor. However, it would have been obvious to modify the device of Nardoni et al. with different types of configurations since Applicants have presented no explanation that this particular configuration of "the ceiling plate section which are arranged on both end sides in a front-rear direction of the shielding conductor project from both side ends of the chip part, and an electromagnetic wave absorber is disposed between at least from the both side ends in a front-rear direction of the chip part to the both side ends in a front-rear direction of the shielding conductor" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al. to the claimed configuration of the ceiling plate section which are arranged on both end sides in a front-rear direction of the shielding conductor project from both side ends of the chip part, and an electromagnetic wave absorber is disposed between at least from the both side ends in a front-rear

direction of the chip part to the both side ends in a front-rear direction of the shielding conductor. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

Re claim 4, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that the chip part includes a two-terminal chip part. However, it would have been obvious to modify the device of Nardoni et al. with different types of configurations since Applicants have presented no explanation that this particular configuration of "the chip part includes a two-terminal chip part" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al. to the claimed configuration of the chip part that includes a two-terminal chip part. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

Re claim 5, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that the shielding conductor width W is selected to have a size larger than an area in which terminals of the chip part exist, by at least twice a harmonic mean of height H of the ceiling plate section and length L of the opening in the horizontal direction of the ceiling plate section. However, it would have been an obvious matter of design choice to use the shielding conductor width W that is selected to have a size larger than an area in which terminals of the chip part exist, by at least twice a harmonic mean of height H of the ceiling plate section and length L of the opening in the horizontal direction of the ceiling

plate section in order to provide specified size of the device, since such a modification would have involved a mere change in the dimensions or proportion of a component. A change in dimensions or proportion is generally recognized as being within the level of ordinary skill in the art. *In Gardner v. TEC Systems, Inc.*, 725 F .2d 1338, 220 USPQ 777 (Fed. Cir. 1984).

Re claim 8, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that a hole section is formed in the ceiling plate section of the shielding conductor to expose the chip part. However, it would have been obvious to modify the device of Nardoni et al. with different types of configurations since Applicants have presented no explanation that this particular configuration of "a hole section is formed in the ceiling plate section of the shielding conductor to expose the chip part" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al. to the claimed configuration of a hole section that is formed in the ceiling plate section of the shielding conductor to expose the chip part. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

Re claim 9, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that a spring substance having elasticity is used as the shielding conductor. Examiner takes official notice that stainless steel and phosphor bronze are well known materials for use in the electrical applications. It would have been obvious to one having ordinary skill in the art at the

time the invention was made to use a spring substance having elasticity as the shielding conductor, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Re claim 10, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that shape memory metal having a characteristic of a spring is used as the shielding conductor, a hole section is formed in the shape memory metal to expose the chip part, and the chip part is pushed by the characteristic of a spring of end sections of the hole section. Examiner takes official notice that Nickel-titanium is a well-known material for use in the electrical applications. It would have been obvious to one having ordinary skill in the art at the time the invention was made to use a shape memory metal having a characteristic of a spring used as the shielding conductor, a hole section formed in the shape memory metal to expose the chip part, and the chip part is pushed by the characteristic of a spring of end sections of the hole section, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. *In re Leshin*, 125 USPQ 416.

Re claim 13, Nardoni et al. substantially discloses an electronic device as set forth in claim 1 above. Nardoni et al. does not explicitly disclose that an array-shaped chip part is used in place of the chip part and the array-shaped chip part includes a plurality of two-terminal chip parts integrated in a front-rear direction. However, it would have been obvious to modify the device of Nardoni et al. with different types of

configurations since Applicants have presented no explanation that this particular configuration of "an array-shaped chip part is used in place of the chip part and the array-shaped chip part includes a plurality of two-terminal chip parts integrated in a front-rear direction" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al. to the claimed configuration of an array-shaped chip part used in place of the chip part and the array-shaped chip part includes a plurality of two-terminal chip parts integrated in a front-rear direction. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

Re claim 14, note that Nardoni et al. discloses two electrodes are formed on a mounting surface of the two-terminal chip part and both of the electrodes are connected to surface layer electric wiring formed in the horizontal direction (see figures 2 and 3).

16. Claims 11, 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nardoni et al. in view of JP2940478 (from hereto referred to as 478).

Re claim 11, the device of Nardoni et al. discloses device as set forth in claim 1 above. It does not explicitly disclose that a shielding conductor also serving as a cathode conductor is used in place of the shielding conductor, and the upper surface, side surfaces, and a part of surfaces of the chip part are covered by the shielding conductor also serving as a cathode conductor. However, 478 teaches of a shielding conductor also serving as a cathode conductor which is used in place of the shielding conductor, and the upper surface, side surfaces, and a part of surfaces of the chip part

are covered by the shielding conductor also serving as a cathode conductor (see figure2). It would have been obvious to one having ordinary skill in the art at the time the invention was made to use the cathode conductor of 478 on electrical device of Nardoni et al. in order to connect the chip and the shielding conductor.

Claim 15, Nardoni et al./478 substantially discloses an electronic device as set forth in claim 11 above. Nardoni et al./478 does not explicitly disclose that on a mounting surface of each of a plurality of two-terminal chip parts, only one of the electrodes is formed. However, it would have been obvious to modify the device of Nardoni et al./478 with different types of configurations since Applicants have presented no explanation that this particular configuration of "on a mounting surface of each of a plurality of two-terminal chip parts, only one of the electrodes is formed" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al./478 to the claimed configuration of on a mounting surface of each of a plurality of two-terminal chip parts, only one of the electrodes is formed. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

Claim 16, Nardoni et al./478 substantially discloses an electronic device as set forth in claim 15 above. Nardoni et al./478 does not explicitly disclose that one of the electrode is connected to surface layer electric wiring formed in the horizontal direction and an optical waveguide is arranged in the horizontal direction in the mounting substrate below the array-shaped chip. However, it would have been obvious to modify

the device of Nardoni et al./478 with different types of configurations since Applicants have presented no explanation that this particular configuration of "one of the electrode is connected to surface layer electric wiring formed in the horizontal direction and an optical waveguide is arranged in the horizontal direction in the mounting substrate below the array-shaped chip" is significant or is anything more than one of numerous configurations. A person having ordinary skill in the art would have found it obvious to modify the device of Nardoni et al./478 to the claimed configuration of one of the electrode that is connected to surface layer electric wiring formed in the horizontal direction and an optical waveguide is arranged in the horizontal direction in the mounting substrate below the array-shaped chip. A change in shape or configuration is generally recognized as being within the level of ordinary skill in the art. *In re Daily*, 149 USPQ 47 (CCPA 1976).

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jinhee J Lee whose telephone number is 571-272-1977. The examiner can normally be reached on M, T, Th and F at 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dean A Reichard can be reached on 571-272-2800 ext. 31. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jinhee J Lee
Patent Examiner
Art Unit 2831

jjl